Nakamura ("Nakamura"). The Examiner stated that Nakamura discloses a vertical MOS transistor in Fig. 22 comprising a semiconductor substrate 1b having a first conductivity type, an epitaxial growth layer 1 having the first conductivity type formed on the substrate, a body region 2 having a second conductivity type formed on the epitaxial layer, a trench 4, a gate insulating film formed in the trench, a polycrystalline silicon gate 22 partially filling the trench and a second gate material 11 filling a remaining part of the trench not filled by the polycrystalline silicon gate 22 and being surrounded thereby and by the gate insulating film.

By the present response, claim 1 has been amended in the manner suggested by the Examiner to overcome the objection thereto. Claims 19 and 20 have been canceled.

Applicant respectfully submits that claims 1 and 10-18 patentably distinguish over the prior art of record.

The present invention relates to an improved vertical MOS transistor structure. As set forth by amended independent claim 1 and independent claim 10, the inventive vertical MOS transistor has a first conductivity type semiconductor substrate, a first conductivity type epitaxial layer formed on the substrate, a second conductivity type body region formed on the epitaxial layer, a trench formed through the body region to extend into the epitaxial layer, a gate insulator formed in the gate, and a gate formed in the trench.

As further recited by independent claims 1 and 10, the gate is comprised of a gate insulating film formed in the trench, a polycrystalline silicon gate (claim 1) or a first gate material (claim 10) partially filling the trench, and a second gate material formed in a remaining portion of the trench not filled by the first gate material or polycrystalline silicon gate. <u>The second gate material is surrounded by the first gate material (or polycrystalline silicon gate) and the gate insulator</u>.

Claim 1 further recites that the second gate material is one of silicon oxide and silicon nitride.

The inventive vertical MOS transistor has a first conductivity type source region formed in an upper surface of the body region surrounding the trench, a gate electrode connected to the gate, a source electrode connected to the source region and drain electrode connected to the semiconductor substrate.

Accordingly, the inventive vertical MOS transistor recited by independent claims 1 and 10 has a trench formed through a second conductivity body region and an epitaxial layer having the first conductivity type formed directly on a first conductivity type substrate. The gate fills the trench and is formed of first and second gate materials which comprise polycrystalline silicon (claim 1) and an insulating

material (claim 10) such as one of silicon oxide and silicon nitride (claim 1).

The claimed invention is disclosed, for example, in the embodiment illustrated in Fig. 11 of the application drawings. The vertical MOS transistor includes a first conductivity type semiconductor substrate 1, a first conductivity type epitaxial layer 2 formed on the substrate 1, and a second conductivity type body region 3 formed on the epitaxial layer 2. A U-shaped trench 4 is formed through the body region 3 to extend into the epitaxial layer 2. A gate oxide film 5 is formed on the side wall and bottom wall of the trench 4. A polysilicon gate 6 partially fills the trench so as to be surrounded by the gate oxide film 5. A silicon nitride or silicon oxide film 12 fills the portion of the trench not filled by the polysilicon gate 6 <u>so as to be surrounded by the gate oxide film 5 and the polysilicon gate 6</u>. A gate electrode 9a is connected to the polysilicon gate material. A source region 7 is formed in the body region 3 to surround the trench 4. A source electrode 7a is connected to the source region 7 and a drain electrode 1a is connected to the substrate 1.

Nakamura was cited as disclosing all elements of the claimed invention, including the silicon nitride or silicon oxide film filling the portion of the trench not

filled by the polysilicon gate 6 so as to be surrounded by the gate insulator and the polysilicon gate.

However, the "second gate material" or insulative film 11 shown in Fig. 22 of Nakamura is clearly not surrounded by either the gate oxide film 9 or the polysilicon gate 22, and the Examiner's reliance on Fig. 5C as demonstrating these limitations of claims 1 and 10 is misplaced. Fig. 5C of Nakamura illustrates one step in a disclosed method of forming a transistor which has the structure shown in Fig. 5A, which is similar to that shown in Fig. 22, wherein the oxide film 11 merely serves to cover and not surround the polysilicon gate 22. The drawings clearly illustrate that the polysilicon gate 22 is in contact with but does not surround the oxide film 11.

Anticipation requires the disclosure, by a single reference, of all claimed subject matter. In the absence of any disclosure of a second gate material surrounded by a polycrystalline gate as required by each of independent claims 1 and 10, anticipation cannot be found. See, e.g., W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) ("Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration"); Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1748 (Fed. Cir. 1991) ("When more than one reference is required to establish

unpatentability of the claimed invention anticipation under § 102 can not be found"); and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added) ("Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim").

The oxide film 11 of Nakamura Fig. 22 is not surrounded by the polysilicon gate 22, and nothing in Nakamura suggests that Fig. 5C "further" illustrates the surrounding nature of the polysilicon gate 22, as contended by the Examiner, or that Fig. 5C is an alternate embodiment in which the polysilicon gate 22 "surrounds" the oxide film 11. In fact, Nakamura explicitly teaches the contrary. At col. 7, lines 27 et seq., Nakamura states that Figs. 1-5 are cross-sectional views showing a step-by-step method of forming a trench MOS gate portion 132, and that Fig. 5C illustrates an orthogonal view of the transistor shown in Fig. 5A. Fig. 5C does not show the polysilicon gate 22 "surrounding" the oxide 11, and merely shows that in a widthwise direction of the transistor, the respective films are recessed due to the presence of a he trench.

Accordingly, applicant respectfully submits that claims 1 and 10-18 are not anticipated by Nakamura and that the rejection under 35 U.S.C. §102(e) should be withdrawn.

Since claims 19 and 20 have been canceled, the rejection under 35 U.S.C. §112 should also be withdrawn.

In view of the foregoing amendments and discussion, the application is now believed to be in condition for allowance. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Twice Amended) A vertical MOS transistor comprising:

a semiconductor substrate having a first conductivity type;

an epitaxial growth layer having the first conductivity type formed on the semiconductor substrate;

a body region having a second conductivity type formed on the epitaxial growth layer;

a trench formed through the body region of the second conductivity type so as to reach inside of the epitaxial growth layer of the first conductivity type;

a gate insulating film formed along an upper surface of the body region of the second conductivity type and a wall surface and a bottom surface of the trench;

a polycrystalline silicon gate partially filling the trench so as to be in contact with the gate insulating film and surrounded by the gate insulating film;

a second gate <u>material</u> comprised of one of a silicon oxide film and a silicon nitride film filling a remaining portion of the trench not filled by the polycrystalline

silicon gate so as to be in contact with the polycrystalline silicon gate and surrounded by the gate insulating film and the polycrystalline silicon gate;

a source region of the first conductivity type formed in the upper surface of the body region of the second conductivity type and around the trench so as to be in contact with the gate insulating film;

a gate electrode connected to the polycrystalline silicon gate and the second gate material;

a source electrode connected to the source region; and

a drain electrode connected to the semiconductor substrate.